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10/627,976	07/28/2003	Anne Kaszynski	T2147-908627	4095

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EXAMINER	
ALHIJA, SAIF A	

ART UNIT	PAPER NUMBER
2128	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/627,976	KASZYNSKI ET AL.	
	Examiner	Art Unit	
	Saif A. Alhija	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 September 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *48-72* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *48-72* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 48-72 have been presented for examination.

Claims 21-47 have been cancelled.

Response to Arguments

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 20 September 2007 has been entered.

i) Applicant's arguments filed 20 September 2007 have been fully considered but they are not persuasive.

ii) It is extremely difficult to ascertain the metes and bounds of the claims. As the Examiner stated previously, the claims appear to be a literal translation from another language and further supplied numerous 112 2nd rejections in order to Applicants to more properly present their claimed invention. Applicants amendments have not resolved the issue and in fact in some cases Applicants amendments have made the claim even less intelligible. At present the first limitation of claim 1 contains no less than 8 commas which makes it extremely difficult to ascertain which limitations and which elements are drawn to each other or their respective explanations. Applicants preamble which is generally not afforded patentable weight is no less than 6 lines. Rather than present another litany of 112 2nd rejections, Applicants are respectfully requested to clarify the claimed invention, either by separating elements and explicitly defining them or through another means which will resolve the confusion in determining Applicants claimed invention. Applicants amendments have resolved a certain number of the specific 112 2nd rejections however some arguments were not found persuasive and the rejections are presented below.

iii) At present the Examiner has not been persuaded that the Killian or Lin references do not anticipate Applicants claimed limitations. Applicants merely argue by reiterating the claimed limitations, summarizing the Killian and Lin references into about 2 lines each then once again reiterating the claimed limitations.

Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references.

Applicant's arguments do not comply with 37 CFR 1.111(c) because they do not clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. Further, they do not show how the amendments avoid such references or objections.

Applicants are once again respectfully requested to more clearly, precisely, and explicitly define Applicants claimed invention in order to expedite prosecution and to avoid the numerous speculative assumptions that would be required by the Examiner in order to most basically determine Applicants claimed invention. Applicants are further requested to focus their explanation on the functionality of the claimed limitations rather than merely reiterating the claimed limitations which lead to speculative assumptions for undefined phrases such as "environment emulator debug mode" and "language adaptation device."

iv) The Examiner maintains the 101 rejections presented in the previous office action, see below. The Examiner withdraws the 112 1st rejections following Applicants amendments.

v) Examiner has cited particular columns and line numbers in the references applied to the claims for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in their entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

vi) The Examiner respectfully requests, in the event the Applicants choose to amend or add new claims, that such claims and their limitations be directly mapped to the specification, which provides support for the subject matter. This will assist in expediting compact prosecution.

vii) Further, the Examiner respectfully encourages Applicants to direct the specificity of their response with regards to this office action to the broadest reasonable interpretation of the claims as presented. This will avoid issues that would delay prosecution such as limitations not explicitly presented in the claims, intended use

statements that carry no patentable weight, mere allegations of patentability, and novelty that is not clearly expressed.

PRIORITY

3. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d).

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

MPEP 2106 recites:

> The claimed invention as a whole must accomplish a practical application. That is, it must produce a "useful, concrete and tangible result" State Street 149 F.3d at 1373, 47 USPQ2d at 1601-02. A process that consists solely of the manipulation of an abstract idea is not concrete or tangibles. See In re Warmerdam, 33 F.3d 1354, 1360, 31 USPQ2d 1754, 1759 (Fed.Cir. 1994). See also Schrader, 22 F.3d at 295, 30 USPQ2d at 1459.

4. **Claims 48-72 are rejected** under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

i) Following Applicants amendment which recites "wherein the environment emulator debug mode and the verification mode are capable of being performed in parallel with the generation of a production file for the ASIC." It is noted that a mere capability is not considered a limitation and is therefore not afforded patentable weight. The claims as presented have not overcome the 101 rejection cited previously. The claims still do not produce a useful, concrete, and tangible result. The claims merely recite the creation, integration, and validation of software however the steps do not culminate with a tangible result. It is further unclear how, assuming the intended use is resolved, would the concept of parallel execution with the generation of a file produce a useful, concrete, and tangible result since it is unclear if the production file is the intended resultant of the claims or merely a tangential

result of the execution of the preceding steps. Further it is unclear what is done with the file itself, stored, displayed, provided to a user, etc.

Appropriate correction is required.

All claims dependent upon a rejected base claim are rejected by virtue of their dependency.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 48-72 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

i) The claims are generally narrative and indefinite, failing to conform with current U.S. practice. They appear to be a literal translation into English from a foreign document and are replete with grammatical and idiomatic errors. See section 2.ii above.

ii) Claims 48 and 71 recite, "replacing at least by a language adaptation device, the software model ... with a high level language abstract description." Claims 48 and 71 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01. The omitted steps are: how the software model is replaced with a high-level language abstract description. Applicants amendment has merely provided a named device which is intended to carry out this replacing however the question posed by the Examiner and repeated in the previous sentence has not been addressed. Therefore the 112 2nd rejection is maintained.

iii) Claims 62 and 63 recite the phrases "readjusting incorrect predictions, reducing the number of valid hypotheses, and terminating collisions." However neither an explanation of how these phrases are accomplished nor a definition of their meaning is provided which renders the claims vague and indefinite. Applicants, in their response, are attempting to impart limitations from the specification into the claims. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., readjusting incorrect predictions, reducing the number of valid hypotheses, and terminating collisions as per Applicants specification) are not recited in the rejected claim(s). Although the

claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Appropriate correction is required.

All claims dependent upon a rejected base claim are rejected by virtue of their dependency.

Claim Objections

6. As stated in MPEP Section 2143.03. A claim limitation which is considered indefinite cannot be disregarded. If a claim is subject to more than one interpretation, at least one of which would render the claim unpatentable over the prior art, the examiner should reject the claim as indefinite under 35 U.S.C. 112, second paragraph (see MPEP § 706.03(d)) and should reject the claim over the prior art based on the interpretation of the claim that renders the prior art applicable. Ex parte Ionescu, 222 USPQ 537 (Bd. Pat. App. & Inter. 1984) (Claims on appeal were rejected on indefiniteness grounds only; the rejection was reversed and the case remanded to the examiner for consideration of pertinent prior art.). Compare In re Wilson, 424 F.2d 1382, 165 USPQ 494 (CCPA 1970) (if no reasonably definite meaning can be ascribed to certain claim language, the claim is indefinite, not obvious) and In re Steele, 305 F.2d 859,134 USPQ 292 (CCPA 1962) (it is improper to rely on speculative assumptions regarding the meaning of a claim and then base a rejection under 35 U.S.C. 103 on these assumptions). It is extremely difficult to ascertain the metes and bounds of the claims. See Section 2.ii above.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7 **Claims 48-72 are rejected** under 35 U.S.C. 102(e) as being clearly anticipated by **Killian et al. "Automated Processor Generation System for Designing a Configurable Processor and Method for the Same", U.S. Patent No. 6,477,683, hereafter referred to as Killian.**

8. **Claims 48-72 are rejected** under 35 U.S.C. 102(e) as being clearly anticipated by **Lin et al. "Converification System and Method", U.S. Patent No. 6,389,379, hereafter referred to as Lin.**

Regarding Claim 48:

The references disclose A method for on demand functional verification of a software model of an application specific integrated circuit (ASIC), wherein said software model is written in a low-level programming language and wherein the method separately establishes said software model and functional verification tests to be applied to the software model for constituting a verification platform comprising an environment emulator debug mode and a verification mode, the method comprising:

creating, in the environment emulator debug mode, an autonomous circuit emulator built around a data processing system, receiving in memory functional specification data obtained by replacing, at least by a language adaptation device, the software model that physically describes the ASIC comprising a circuit under design to be validated, with a high level language abstract description, the autonomous circuit emulator generating response data structures in accordance with said functional specification data, as a function of stimuli received from an environment emulator;

(Killian. Abstract. Figure 6. Column 35, Lines 1-22)

(Lin. Column 18, Lines 1 – Column 19, Line 4.)

integrating the software model into a verification platform, and connecting the previously validated autonomous circuit emulator in parallel to interfaces of the software model connected to said environment emulator;

(Killian. Abstract. Automated Processor Design Tool)

(Lin. Column 21, Line 34 – Column 22, Line 11.)

utilizing the verification platform in the verification mode, by comparing response data from interfaces of the software model with the response data structures taken as a reference for the validation of response data transmitted by the software model;

(Killian. Abstract. Testing to optimize processor implementation)

(Lin. Column 27, Lines 45-67)

and validating the software model or invalidating the software model by outputting one or more error notifications when the response data of the software model are not identical to the response data structures,

(Killian. Column 40, Lines 15-18)

(Lin. Column 124, Lines 25-52)

wherein the environment emulator debug mode and the verification mode are capable of being performed in parallel with the generation of a production file for the ASIC.

(Examiners Note. A capability is not considered a limitation and is therefore not afforded patentable weight.)

(Killian. Figure 12, Parallel Data Unit Execution)

(Lin. Column 4, Lines 41-54. Parallel Design)

Regarding Claim 49:

The references disclose A method according to claim 48, wherein the autonomous circuit emulator generates the response data structures, in response to a user input, which correspond to the functional specification of the software model of the ASIC, the method further comprising;

writing the functional specification data and storing in the verification platform, a test program for testing the software model of the ASIC, comprising input stimuli sequences to be provided to the software model of the ASIC, related to output stimuli sequences generated by the autonomous circuit emulator, based on the functional specification data;

linking together and activating the autonomous circuit emulator and the verification platform; and

comparing output stimuli of both the response data of the software model of the ASIC and the response data structures, wherein the software model of the ASIC is a Hardware Description Language (HDL)-type model, in order to functionally validate the software model of the ASIC by the test program, and thus validating the software model in relation to the functional specification data.

(See rejection for claim 48)

Regarding Claim 50:

The references disclose A method according to claim 48, wherein the autonomous circuit emulator communicates with a user to control the activation of previously created and stored models of input stimuli sequences defined in a high- level programming language, and controls the activation of associated programs for the progressive validation of test sequences determined from the models.

(Killian. Column 8, Lines 9-43. Column 9, Line 37 – Column 10, Line 67. Column 23, Lines 21-45)

(Lin. Figure 1, Elements 20, 30, and 40)

Regarding Claim 51:

The references disclose A method according to claim 48, wherein the functional specification data comprise a sequence of instructions in a low-level programming language, specifying functional models of circuits.

(Killian. Column 8, Lines 9-43. Column 9, Line 37 – Column 10, Line 67. Column 23, Lines 21-45)

(Lin. Figure 1, Elements 20, 30, and 40)

Regarding Claim 52:

The references disclose A method according to claim 48, wherein the functional specification data are provided in the form of a first specification program in a low level programming language of functional models of circuits, and a second specification program in a high level programming language of functional models of circuits, and the autonomous circuit emulator performs a co-simulation by synchronizing the execution of the first and second specification programs.

(Killian. Column 8, Lines 9-43. Column 9, Line 37 – Column 10, Line 67. Column 35, Lines 1-22)

(Lin. Figure 3, Elements 210, 215, and 220)

Regarding Claim 53:

The references disclose A method according to claim 52, wherein the low level language is a Hardware Description Language (HDL)-type and the high level language is C++.

(Killian. Column 8, Lines 9-43. Column 9, Line 37 – Column 10, Line 67. Column 35, Lines 1-22)

(Lin. Figure 3, Elements 210, 215, and 220)

Regarding Claim 54:

The references disclose A method according to claim 48, wherein the verification platform verifies that the responses of the software model of the ASIC are within response time ranges specified in the functional specification data.

(Killian. Figure 2. Element 84)

(Lin. Column 2, Lines 20-40)

Regarding Claim 55:

The references disclose A verification platform for on demand verification of a software model of an application specific integrated circuit (ASIC), comprising a data processing system receiving selection requests from a client to select test models producing input stimuli applied to the software model of the ASIC, said data processing system comprising in memory functional specification elements of the ASIC which are read in a high level language and comprising in memory a sequence of programmed instructions of an emulator program that generates output stimuli of a functional validation test program, in relation to the input stimuli and the functional specification elements, wherein a comparator compares the output stimuli of the functional validation test program with output stimuli of the software model and wherein one or more error notifications are output when compared output stimuli are not identical, wherein the environment emulator debug mode and the verification mode are capable of being performed in parallel with the generation of a production file for the ASIC. **(See rejection for claim 48)**

Regarding Claim 56:

The references disclose A verification platform according to claim 55, further comprising a library of functional models of circuit blocks for a plurality of ASICs and means for selecting models through a definition file of the integrated circuit configuration, for creating a model corresponding to the functional specification of one of said plurality of ASICs that is integrated into the definition of an environment of the ASIC.

(Killian. Column 8, Lines 9-43. Column 23, Lines 21-45)

(Lin. Figure 1, Elements 20, 30, and 40)

Regarding Claim 57:

The references disclose A verification platform according to claim 55, further including, in a link connecting the platform to a client, first and second serial programming language adaptation circuits, wherein the first serial programming language adaptation circuit transforms commands in a high level programming language used by the client into commands in a low level programming language used by the ASIC model, and wherein the second serial programming language adaptation circuit transforms the commands in the low level programming language back into commands in the high level programming language.

(Killian. Column 9, Line 37 – Column 10, Line 67.)

(Lin. Figure 3, Elements 210, 215, and 220)

Regarding Claim 58:

The references disclose A verification platform according to claim 55, further comprising means for executing operations at the same time as the simulation, and, upon detection of an error notification output, interrupting operations at the time the error notification appears.

(Killian. Figure 2. Element 72)

(Lin. Figure 65 and corresponding description, interrupt handlers)

Regarding Claim 59:

The references disclose A verification platform according to claim 55, wherein the functional specification elements are constituted by a truth table corresponding to the functions of the various functional circuit elements of the ASIC software model, and further comprising a propagation delay associated with each input and each output pair.

(Killian. Table 1. Column 24, Lines 11-22)

(Lin. Figure 1 and 61, Element RD0_0)

Regarding Claim 60:

The references disclose A verification platform according to claim 55, wherein the functional specification elements are constituted by a behaviour table corresponding to the functions of the various functional circuit elements of the ASIC software model, and further comprising a propagation delay associated with each input and each output pair.

(Killian. Table 1. Column 24, Lines 11-22)

(Lin. Figure 1 and 61, Element RD0_0)

Regarding Claim 61:

The references disclose A verification platform according to claim 55, further including a cache memory for storing the blocks used by nodes according to node addresses, and means for managing, for an address used by one or more nodes, a presence vector with one presence indicator per node.

(Killian, Column 19, Lines 47-57)

Regarding Claim 62:

The references disclose A verification platform according to claim 61, wherein the programmed instructions are object-oriented and the emulator is structured as a set of classes for managing a collection of execution hypotheses for a transaction in a memory block of the software model, and for managing transactions that are concurrently colliding using the same memory block.

(Killian. Column 12, Lines 10-20)

Regarding Claim 63:

The references disclose A verification platform according to claim 61, wherein algorithms of the sequence of programmed instructions of the emulator are configured to cause the emulator to perform functions comprising generating predictions, eliminating predictions, readjusting incorrect predictions, reducing the number of valid hypotheses, and terminating collisions.

Regarding Claim 64:

The references disclose A verification platform according to claim 63, wherein the emulator of the ASIC circuit generates predictions without having to obtain additional information on the internal operation of the ASIC circuit, the ASIC circuit being a circuit under design.

(Killian. Figure 6)

(Lin. Figure 1 and 3)

Regarding Claim 65:

The references disclose A verification platform according to claim 61, wherein the platform is used as an emulator of a router circuit, a circuit with cache or a router circuit with cache.

(Killian. Figure 6)

(Lin. Figure 1 and 3)

Regarding Claim 66:

The references disclose A verification platform according to claim 61, wherein the platform is configured for testing a software model of an integrated circuit (ASIC) on demand and comprises an ASIC emulator for controlling a comparator that receives values generated by a software model of the ASIC circuit tested, upon reception of stimuli sent by at least one stimuli generating circuit storing a test program, an interface for translating the stimuli from an advanced language into a low level language corresponding to that of the software model, and means for validating the verification in case of the detection of a collision by the comparator.

(Killian. Figure 6)

(Lin. Figure 1 and 3)

Regarding Claim 67:

The references disclose A verification platform according to claim 61, further comprising means for selecting the response to stimuli that depend on the composition of the circuits tested, said means for selecting being

constituted by a model generated by means for selecting functional models from a library, which associates with each of the models the responses to a given stimulus, the model corresponding to the composition of the circuit to be tested.

(Killian. Figure 2)

(Lin. Figure 1 and 3)

Regarding Claim 68:

The references disclose A verification platform according to claim 67, further including means for storing responses selected so as to create a test model to be applied to the circuit tested during the reception of stimuli.

(Killian. Figure 2, element 80)

(Lin. Figure 1 and 3)

Regarding Claim 69:

The references disclose A verification platform according to claim 55, wherein each transaction comprises, at the level of each interface, a request packet and one or more associated response packets, wherein the values of the parameters and/or the transmission time constraints of the request packet and one or more associated response packets can be forced from the functional test program executed by the emulator of the environment, which appropriately translates all of said parameters during the transmission of the request packet and one or more associated response packets to the terminals of the software model of the design.

(Killian. Column 2, Lines 35-49)

(Lin. Column 3, Lines 15-20, Signal)

Regarding Claim 70:

The references disclose A verification platform according to claim 68, wherein the generation of predictions is performed by the emulator of the circuit after receiving information on the internal operation of the circuit, the circuit being a circuit under design.

(Killian. Figure 6)

(Lin. Figure 1 and 3)

Regarding Claim 71:

The references disclose A computer-readable medium upon which is encoded a sequence of programmed instructions that, when executed by a processor, cause the processor to perform a method for on demand functional verification of a software model of an application specific integrated circuit (ASIC), wherein said software model is written in a low-level programming language and wherein the method separately establishes said software model and functional verification tests to be applied to the software model for constituting a verification platform comprising an environment emulator debug mode and a verification mode, the method comprising:

creating, in the environment emulator debug mode, an autonomous circuit emulator built around a data processing system, receiving in memory functional specification data obtained by replacing, at least by a language adaptation device, the software model that physically describes the ASIC comprising a circuit under design to be validated, with a high level language abstract description, the autonomous circuit emulator generating response data structures in accordance with said functional specification data, as a function of stimuli received from an environment emulator;

integrating the software model into the verification platform, and connecting the previously validated autonomous circuit emulator in parallel to interfaces of the software model connected to said environment emulator;

utilizing the verification platform in the verification mode, by comparing response data from interfaces of the software model with the response data structures taken as a reference for the validation of response data transmitted by the software model; and

validating the software model or invalidating the software model by outputting one or more error notifications when the response data of the software model are not identical to the response data structures

wherein the environment emulator debug mode and the verification mode are capable of being performed in parallel with the generation of a production file for the ASIC.

(See rejection for claim 48)

Regarding Claim 72:

The references disclose A computer readable medium according to claim 71, further comprising programmed instructions for:

generating, using a data processing system and in response to a user input, the autonomous circuit emulator which provides a simulation configuration corresponding to the software model of the ASIC using the functional specification;

writing the functional specification data and storing in the verification platform a test program for testing the software model of the ASIC, comprising input stimuli sequences to be provided to the software model of the ASIC, related to output stimuli sequences generated by the autonomous circuit emulator, based on the functional specification data;

linking together and activating the autonomous circuit emulator and the verification platform; and

comparing output stimuli of both the response data of the software model of the ASIC and the response data structures, wherein the software model of the ASIC is a Hardware Description Language (HDL)-type model, in order to functionally validate the software model of the ASIC by the test program, and thus validating the software model in relation to the functional specification data.

(See rejection for claim 48)

Conclusion

9. All Claims are rejected.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saif A. Alhija whose telephone number is (571) 272-8635. The examiner can normally be reached on M-F, 11:00-7:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on (571) 272-22792279. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SAA

November 23, 2007

KAMINI SHAH
SUPERVISORY PATENT EXAMINER